Supplementary Material for

Phosphorene: A Unexplored 2D Semiconductor with a High Hole Mobility

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1. *Ab initio* Calculations

We determined the equilibrium structure, stability and electronic properties of bulk black phosphorus and few-layer phosphorene using *ab initio* density functional theory (DFT) calculations as implemented in the SIESTA[1] and VASP[2] codes. Few-layer phosphorene crystals have been represented by a periodic array of slabs, separated by a 15 Å thick vacuum region. All structures were optimized using the Perdew-Burke-Ernzerhof (PBE)[3] exchange-correlation functional, norm-conserving Troullier-Martins pseudopotentials[4], and a double-ζ basis including polarization orbitals. The reciprocal space was sampled by a fine *k*-point grid[5] in the Brillouin zone of the primitive unit cell, using the 8×8×2 grid for the bulk and the 8×8×1 grid for few-layer phosphorene. We used a mesh cutoff energy of 180 Ry to determine the self-consistent charge density, which provided us with a precision in total energy of ≤2 meV/atom. This total energy approach and precision requirement is analogous to a recent DFT study of the simple cubic phosphorus structure[6] based on the Local

Density Approximation (LDA) for the exchange-correlation functional.[7,8]

Whereas structural parameters obtained by DFT with PBE and LDA functionals agree generally very well with experimental data, the interpretation of DFT eigenvalues as a representation of quasiparticle energies is dangerous. In comparison to the observed bulk band gap value of 0.31-0.36 eV, DFT values based on LDA and PBE are significantly smaller. The LDA band gap value is negative, suggesting that this system should be metallic, and our PBE band gap value E_g = 0.04 eV, while positive and in agreement with published theoretical results,[9,10] is significantly smaller than the observed value. To reproduce the observed bulk band gap value, we used the Heyd-Scuseria-Ernzerhof (HSE06)[11] hybrid exchange-correlation functional in DFT as implemented in the VASP code.[2] This approach is computationally more demanding than PBE or LDA, but not completely predictive, since the electronic spectrum depends sensitively on the parameter AEXX that describes the mixing between the Hartree-Fock exchange and the PBE exchange-correlation functional. Our results in Fig. 1(e)-(f) of the main manuscript are obtained using the value AEXX=0.04.

2. Temperature Dependent Carrier Mobility

We have also investigated both the field-effect mobility and the Hall mobility of few-layer phosphorene as a function of temperature and present our results in Fig. S1. The measured field-effect mobility on the ~ 8nm thick film is ~ 100 cm^2/Vs, being

consistent with other measured field-effect transistors shown in Fig. 4c. Due to the dependence of the carrier mobility on the crystal orientation of different samples, we normalized the mobility results to the room-temperature value to see the general trend and focus on their dependence on temperature. Our four-terminal mobility measurements, presented in Fig. S1a, show an increase by a factor of 5 of the observed field-effect mobility as the temperature drops from 300K to 10K. In contrast to this finding, our two-terminal measurements, also reproduced in Fig. S1a, show a mobility decrease at lower temperatures. The two-terminal measurements do not represent the intrinsic mobility behavior, but rather reflect the temperature dependence of the contact resistance caused by the Schottky barriers at the metal/phosphorene interface as discussed in the manuscript. We expect the contact resistance to increase and eventually to dominate at lower temperatures, when thermally assisted tunneling is greatly restrained. The apparent discrepancy between these two sets of data confirms the importance of using four-terminal measurements to extract the intrinsic mobility at lower temperatures in order to avoid artifacts associated with contact resistances.

The Hall mobility and carrier density between 100K and room temperature have been measured by the standard Hall technique on the fabricated Hall-bar structured samples with the film thickness ranging from 6 nm to 8 nm, as shown in Fig. S1b and S1c. We have found the room-temperature Hall mobility to be in the same range as the field-effect mobility determined in few-layer phosphorene transistors. We also observed an increase in the Hall mobility at lower temperatures, where

electron-phonon scattering assumes to be suppressed. Since the Hall measurement is, in principle, a 4-terminal measurement, the influence of Schottky contacts should play a less role in the results being consistent with the result shown in Fig. S1a.

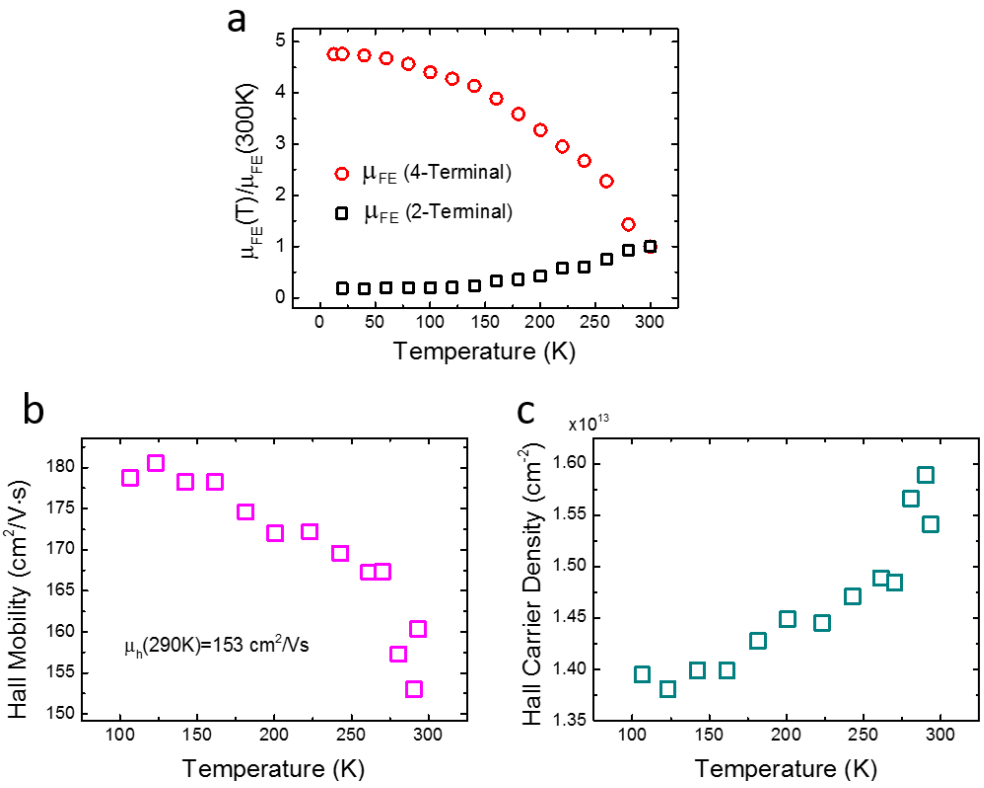

Figure S1 | Field-effect and Hall mobility measurements. a, Temperature-dependent field-effect mobility, **b,** Temperature-dependent Hall mobility and **c,** temperature-dependent Hall carrier density.

3. Determination of Field-effect Mobility

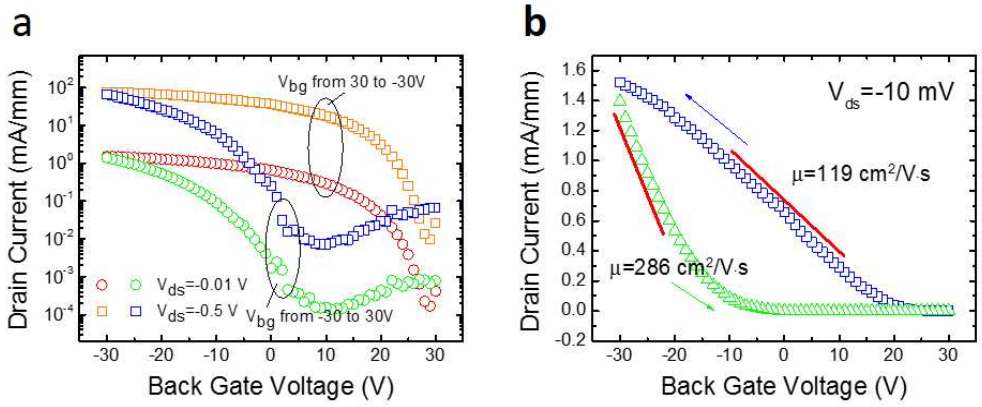

Figure S2 | Hysteresis in back-gated few-layer phosphorene transistors. Transfer curves of a back-gated phosphorene transistor presented on a semi-logarithmic scale (a) and a linear scale (b).

In our experiments, back-gated few-layer phosphorene transistors were used to extract the field-effect mobility. The back-gated devices used the globally heavily doped silicon substrate as the gate and 90 nm SiO_2 as the gate dielectric. Due to the thick dielectric layer and an un-optimized phosphorene/SiO_2 interface, we observed a large hysteresis in bi-directional sweeps of the transfer curves. Though both transfer curves reflect a clear *p*-type transistor performance, a large threshold voltage V_T shift is observed, as seen in Figs. S2a and S2b. The origin of the V_T shift can be mostly attributed to the presence of trapped charges in the dielectric. Because charge traps are charging or discharging at different gate voltages during the sweep from -30 V to +30 V or in the reverse direction, the observed trans-conductance depends on the voltage sweep direction. Therefore, the field-effect mobility, extracted from trans-conductance peak, has different values ignoring trap effects. For the positive

sweep, the maximum field-effect mobility is 286 $cm^2/V{\cdot}s$, whereas it drops to 119 $cm^2/V{\cdot}s$ for the reverse sweep. When the back-gate sweeps from 30V to -30V, all bulk and interface traps need to be slowly filled and eventually holes are strongly accumulated in the few-layer phosphorene film. With the back-gate bias sweeping from -30V to 30V, the accumulated holes are first fast depleted thus the drain current reduces to zero. That's why field-effect mobility extraction is more meaningful determined from fast depletion region which is more associated with channel mobility. Meanwhile, most of 2D transistors field-effect mobility is extracted in this way. It is helpful for us to have an apple to apple comparison of few-layer phosphorene transistors with others.

4. Schottky Barriers in Phosphorene Transistors

Mostly due to lack of source/drain doping, metal contacts on 2D materials usually form considerable Schottky barriers at the metal/semiconductor junction,[12] turning few-layers phosphorene transistors to Schottky transistors instead of conventional MOSFETs. The presence of Schottky barriers is expected to significantly modify the device parameters and to have a strong impact on the device performance based on the following reasoning.

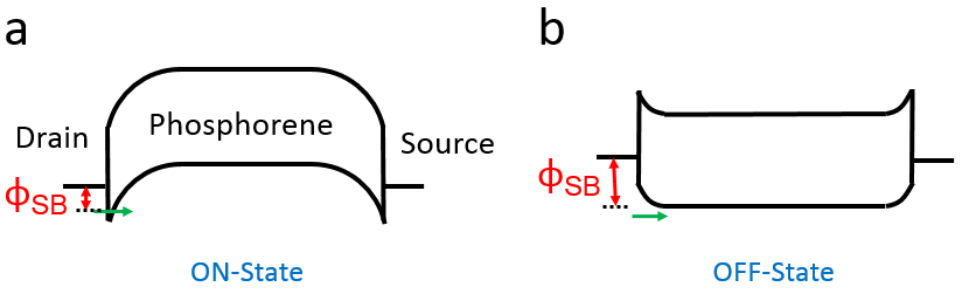

Figure S3 | Band diagram of phosphorene transistors. a, In the ON-State, the Schottky barrier width is greatly reduced. **b,** In the OFF-State, the Schottky barrier height is increased.

(i) As shown in Figure S4, the ON/OFF states in few-layer phosphorene transistors are not completely controlled by the carrier density in the few-layer phosphorene channel, as is the case in Si MOSFETs. Instead, they are dominantly controlled by the effective Schottky barrier for holes. In the ON-State, e.g. at V_{bg}=-30 V, both conduction and valence bands are pushed upwards, leaving a reduced Schottky barrier width, which facilitates the hole injection from the contact metal in a thermally assisted tunneling process. In contrast to this, in the OFF-State, e.g. at V_{bg}=+30 V, both bands are pulled down, thus drastically increasing the barrier height for hole tunneling. Therefore, the hole current is strongly suppressed in this case, while the electron current is possibly increased, as also seen in Fig. S3a. Still, the electron current cannot become as large as the hole current, since the mobility of electrons is lower than that of holes and since few-layer phosphorene is a natural *p*-type semiconductor. Therefore, if we still were to use the Drude model to extract the field-effect mobility, the mobility calculated would be underestimated even in a four-terminal measurement (which eliminates the effect of Schottky barriers), since

the channel could not be modeled as a pure resistor.

(ii) Presence of Schottky barriers at the metal contacts would degrade the performance of transistors and the CMOS inverter as well. In Schottky barrier transistors, it should be more difficult to reach a full saturation of the output curves than in conventional MOSFETs, since a great portion of the drain bias voltage would appear also across the contacts. In conventional Si MOSFET based CMOS inverters, in the ON-state at the vicinity of the switching threshold voltage V_M, both the PMOS and the NMOS are in the saturation region, and the drain current is identical in both transistors. A small change in the V_{in} voltage would require the drain current to change drastically. If the transistor is in the saturation region, it requires a drastic change in the drain bias for either transistors, thus to maintain the same drain current for both PMOS and NMOS channels. This drastic change in the drain bias would show up as a large change in V_{OUT}, leading to a satisfactory value of the inverter gain. However, in Schottky barrier transistors, which can not easily reach the saturation region, a small change in the drain bias would meet the demand. As a result, the gain of such transistors would be significantly reduced. In our 2D CMOS, most gain values are slightly over 1. This is caused by the above-mentioned characteristics of contacts at metal/2D semiconductor interfaces. We expect to be able to improve the device performance by reducing the Schottky barrier height/width. We are convinced that contact engineering becomes one of the most important device aspects in 2D materials and devices research.[13]

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