Nano Letters (2014)

Supplementary Information for

High Mobility WSe_2 *p*- and *n*-Type Field Effect Transistors Contacted by Highly Doped Graphene for Low-Resistance Contacts

Hsun-Jen Chuang, Xuebin Tan, Nirmal Jeevi Ghimire, Meeghage Madusanka Perera Bhim Chamlagain, Mark Ming-Cheng Cheng, Jiaqiang Yan, David Mandrus, David Tománek and Zhixian Zhou

1. Sample preparation and device fabrication

WSe_2 crystals were synthesized by chemical vapor transport using iodine as transport agent. The as-grown crystals were phase-pure as determined by x-ray diffraction. Atomically thin MoS_2 flakes were produced from the bulk crystal by a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrate covered with a 290 nm-thick thermal oxide layer. An optical microscope was used to identify thin flakes, which were further characterized by Park Systems atomic force microscopy (AFM) in the non-contact mode. Thin h-BN crystals (10 - 50 nm thick) were first exfoliated from commercially available h-BN crystals onto a PDMS stamp. Using a home-built precision transfer stage, they were subsequently transferred onto a few-layer WSe_2 flake to cover its middle section while exposing its two ends for electrical contacts. The graphene used in this study was grown on copper using a chemical vapor deposition (CVD) method.[1-3] Briefly, the CVD graphene was grown on a 25 μm thick copper foil (Alfa Aesar) in a mixture of methane and hydrogen at 1000 ^oC. A layer of 200 nm thick Poly(methyl methacrylate) (PMMA) was spin-coated and dried at room temperature. After removing the graphene on the back side of the copper using oxygen plasma, the copper foil was etched away using diluted copper etchant (APS-100) for 24 hours. The PMMA/graphene film was cleaned using a modified RCA cleaning procedure.[2] PMMA/graphene films were transferred onto the silicon substrate with a few-layer WSe_2 sample by carefully scooping it out from the solution. Finally, PMMA was dissolved by acetone. Electron beam lithography and oxygen plasma etching were used to pattern the graphene electrodes. Metal electrodes, consisting of 5 nm of Ti covered by 50 nm of Au, were fabricated to electrically wire up the graphene electrodes using standard electron beam lithography (EBL) and electron

beam deposition. Ionic liquid gate electrodes were also fabricated in the same step. A schematic illustration of the dry transfer process used to passivate the WSe_2 channel with a clean h-BN microcrystal is presented in Figure S1.

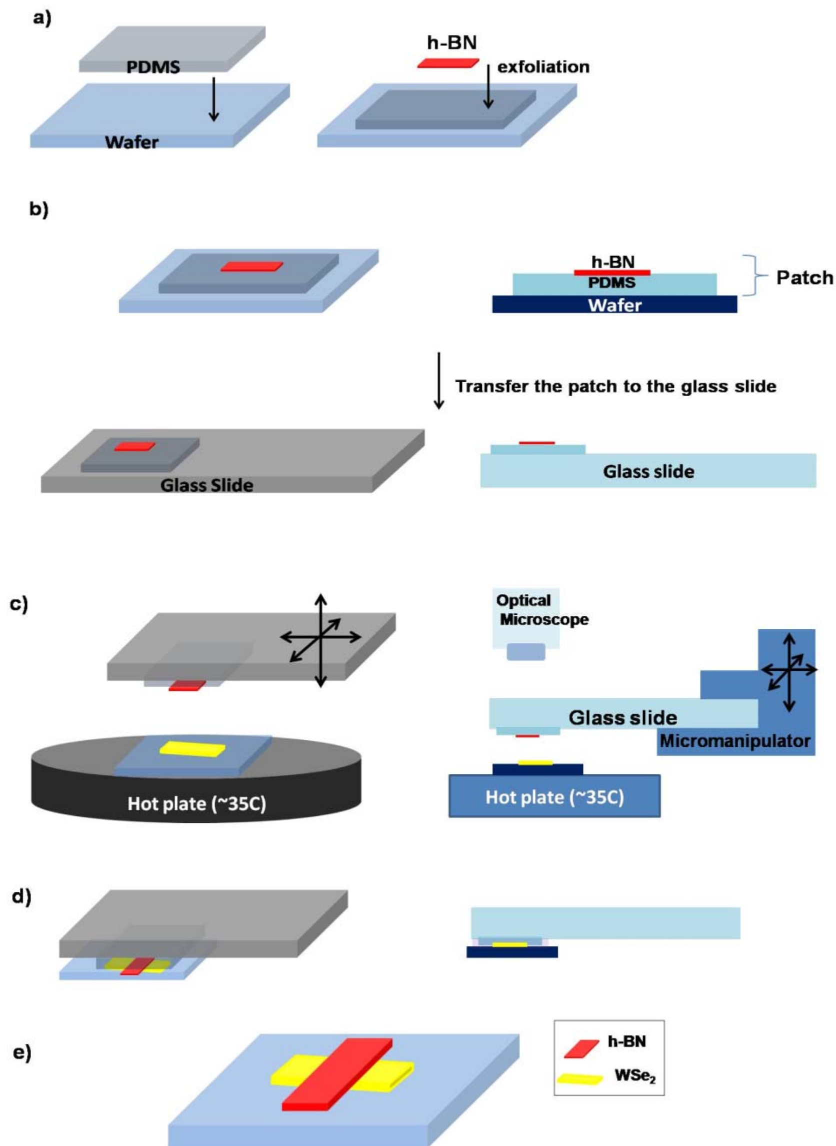

Figure S1. Schematic illustration of the process to cover the WSe_2 channel with a h-BN crystal using a transfer stage equipped with a micromanipulator and a long working distance microscope objective.

2. Transfer characteristics and field-effect mobility of an Al_2O_3 passivated WSe_2 device

For the sake of comparison, we have also measured a graphene-contacted WSe_2 device with its channel passivated with 50 nm of electron beam deposited Al_2O_3. Figures S2a and S2b show the transfer characteristics of the device, while the graphene contacts have been either highly "*p*-doped" by applying a very high ionic liquid (IL) gate voltage of -6 V or "*n*-doped" by applying an IL gate voltage of +6V. Clearly, the threshold voltage for both the hole and electron channels in the Al_2O_3 passivated device is much larger than in the h-BN passivated device shown in Figure 4 of the main manuscript. Figure S2c shows that the field-effect mobility is also much lower in the Al_2O_3 passivated device than in the h-BN passivated device, which can be attributed to additional charge traps and interface roughness introduced by Al_2O_3.

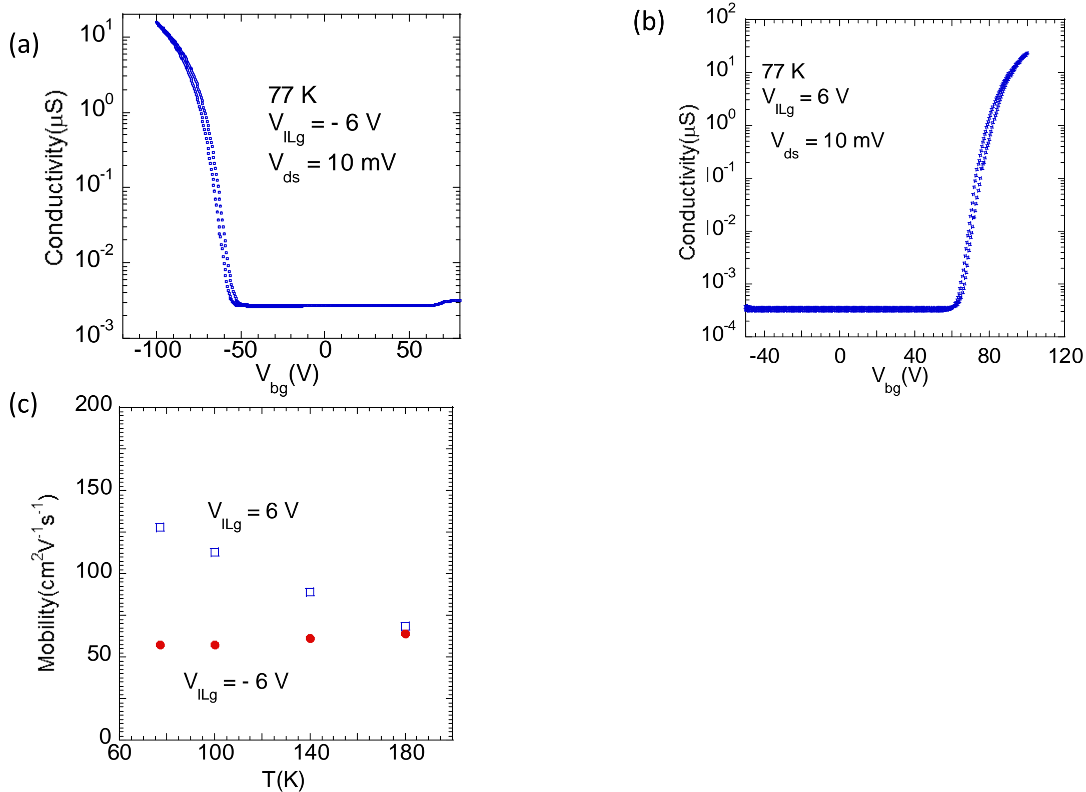

Figure S2 (a-b) Transfer characteristics of a 7 nm thick WSe_2 FETs with ionic-liquid gated graphene contacts, measured at V_{ILg} = -6 V (hole channel) and V_{ILg} = 6 V (electron channel). (c) Field-effect mobility of the devices in the hole- (V_{ILg} = -6 V) and electron-doped (V_{ILg} = 6 V) regions.

3. Output, transfer characteristics and field effect mobility of a bear WSe_2 device

As shown in Figures S3a and S3b, the output characteristics of a 8 nm thick bear, i.e. not passivated WSe_2 channel with IL-gate graphene contacts shows Ohmic behavior. The highest current in this device approaches 200 μA/μm at 4.0 μm channel length at the back-gate voltage V_{bg} = 100 V, drain-source voltage V_{ds}= -5 V, and IL-gate voltage V_{ILg} = -4.5 V. The transfer characteristics of the bear WSe_2 device is qualitatively consistent with that of the h-BN passivated devices. However, the ON/OFF ratio in the bear device is substantially reduced due to the IL-gating of the channel as well, especially at high IL-gate voltages, as seen in Figure S3c. Figures S3e and S3f show the field-effect mobility of the bear WSe_2 device for both the hole and electron channels. The mobility observed in the bear sample is also smaller in comparison to the h-BN passivated device discussed in the main text, further indicating that channel passivation with ultraclean h-BN is critical for studying intrinsic channel properties.

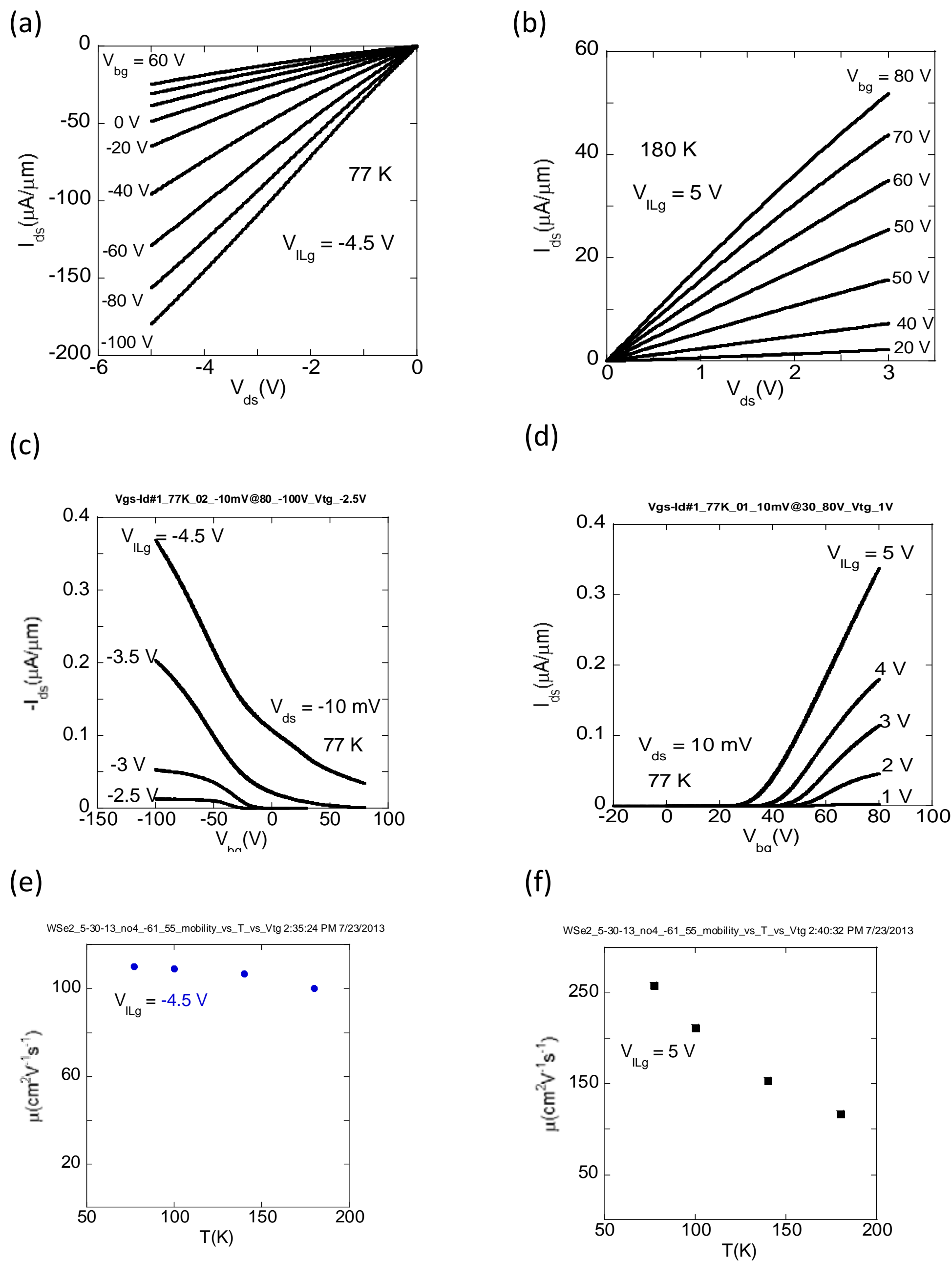

Figure S3. An 8 nm thick WSe_2 FET device with a channel length of L = 4 μm and IL-gated graphene contacts. (a-b) Output characteristics for the hole and electron channels. (c-d) Transfer characteristics for the hole and electron channels. (e-f) Field effect mobility extracted from the low-bias (V_{ds} = 10 mV) transfer characteristics for the hole and electron channels.

4. Estimation of the contact resistance from a short-channel WSe_2 device

Figure S4a shows the output characteristics of a short-channel device (channel length L ≈ 200 nm) with IL-gated graphene contacts. The ON-state resistance of the device, measured at a high IL-gate voltage and a high back-gate voltage in the linear low drain-source voltage region between electrodes labeled 3L and 4 in Figure S4c, is determined to be 5 kΩ. This resistance consists of the metal/graphene contact resistance, the graphene electrode sheet resistance, the WSe_2 channel resistance, and the graphene/WSe_2 contact resistance. To isolate the contact resistance of the graphene/WSe_2 junctions, we also measured the resistance of a graphene sheet and the graphene/metal contacts separately. As shown in Figure S4b, the total resistance measured between electrodes 2L and 2R in Figure S4c is 2.2 kΩ. As suggested by the device layout in Figure S4c, *i*) the total resistance between electrodes 2L and 2R should be comparable to that between electrodes 3L and 3R; and *ii*) the metal/graphene contact resistance and graphene electrode sheet resistance are likely much smaller for electrode 4 than electrode 3L, given the much longer metal/graphene contact length and smaller L/W ratio for electrode 4 than 3L. Therefore, the maximum contact resistance of a graphene/WSe_2 junction is estimated to be $R_c = (R_{ON} - R_{G\text{-}ele})/2 = (5\ k\Omega - 2.2\ k\Omega/2)/2 \approx 2\ k\Omega$. Since the width of this particular WSe_2 sample is 1.0 µm, the normalized contact resistance of the graphene/WSe_2 junction is less than 2 kΩ·µm.

In order to quantitatively study the graphene/WSe_2 junction and the intrinsic WSe_2 channel properties, it is important to minimize the graphene sheet resistance and graphene/metal contact resistance. Low sheet resistance of ~100 Ω/sq has been obtained in monolayer graphene that had been electrostatically doped up to 3×10^{13} cm^{-2} by ferroelectric dipoles[4]. Low metal/graphene contact resistance of the order of 10^2 Ω·µm has been routinely achieved by selecting proper contact metal[5]. The graphene sheet resistance and the graphene/metal contact resistance can be further minimized *(i)* by shaping the graphene electrodes in such a way that the metal/graphene contact area is much larger than that of the graphene/WSe_2 interface, and *(ii)* by electrostatically doping the graphene electrodes up to a very high carrier concentration of ~10^{14} cm^{-2} using an IL.

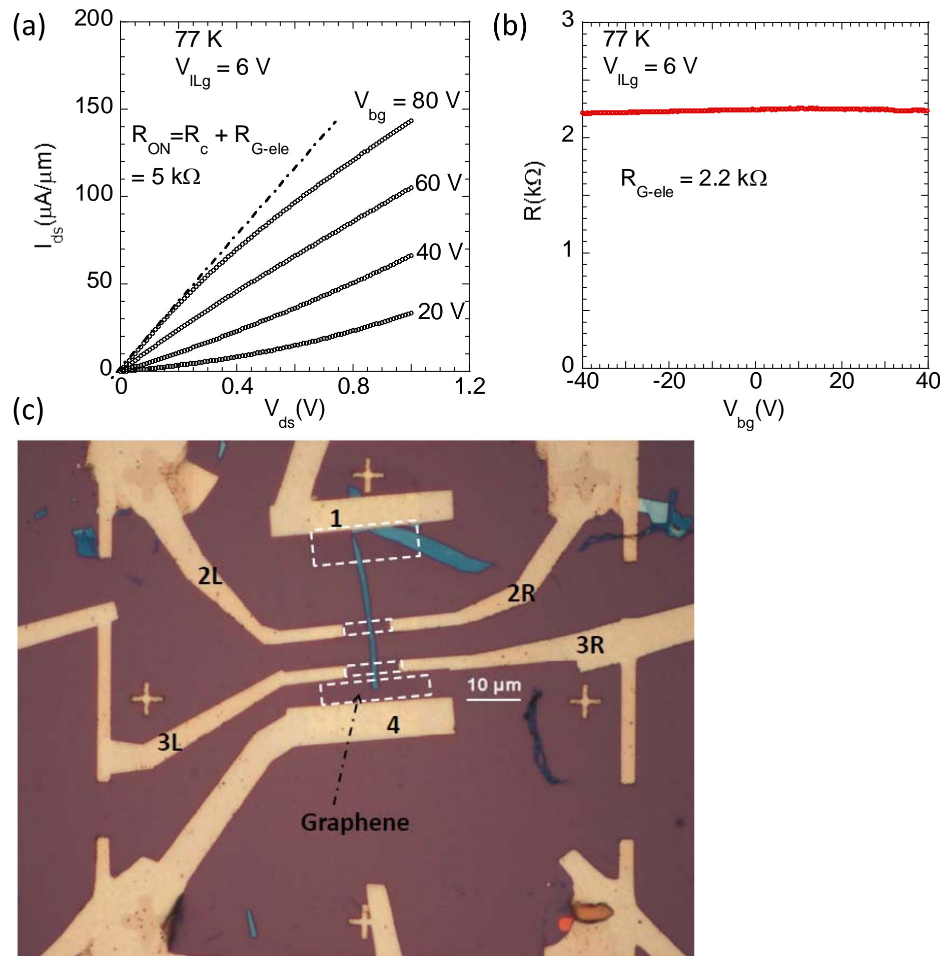

Figure S4. (a) Output characteristics of a short channel (L≈ 200 nm) WSe_2 device shown between electrodes 3L/3R and 4, depicted in panel (c), at a high IL-gate voltage of 6 V. (b) The resistance of a graphene FET device between electrodes 2L and 2R, depicted in panel (c), at a high IL-gate voltage of 6 V. (c) Optical micrograph of a 8 nm think WSe_2 sample contacted by graphene electrodes in the area highlighted by the white dashed lines. The channel length between electrodes 3L/3R and 4 is about 200 nm.

5. Conductance *versus* back-gate voltage curves corresponding to the opposite sweeping directions of a double-sweep measurement

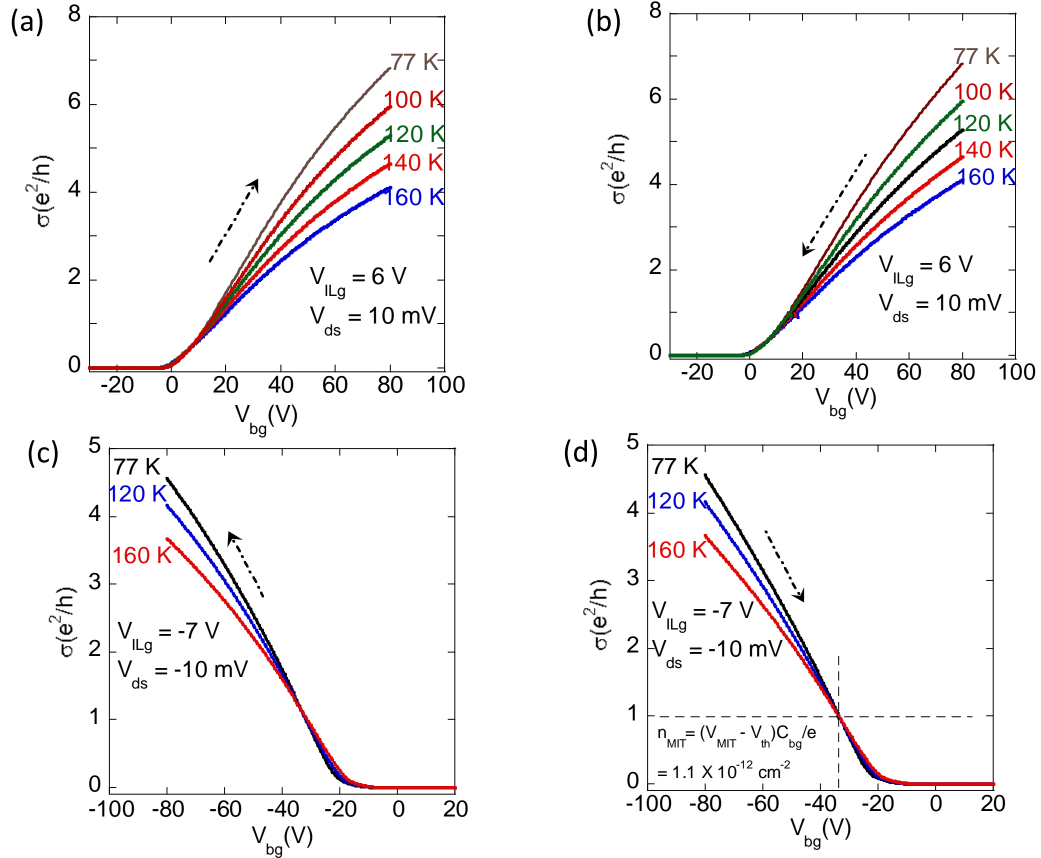

Figure S5. Temperature dependent two-terminal conductivity as a function of the gate voltage for the WSe_2 device shown in Figure 2 of the main text with dual-gate sweep directions, obtained after it was cooled down from 230 K at the IL gate voltages (a-b) V_{ILg} = 6 V and (c-d) V_{ILg} = -7 V. The direction of the gate sweep is indicated by the arrow in the figure.

6. Transfer characteristics of a graphene FET on WSe_2 substrate.

Field-effect mobility is extracted from the V_{bg} dependence of σ using the expression $\mu=(1/C_{bg})\times(d\sigma/ dV_{bg})$ in the linear region of the σ *vs* V_{bg} curves, where C_{bg} is the back-gate capacitance per unit area. Based on a simple parallel-plate capacitor model, C_{bg} is determined to be 1.2 $\times10^{-8}$ F cm^{-2} for 290 nm SiO_2 (C_{bg} =

$3.9\times\varepsilon_0/290$ nm). We have previously shown that the IL deposited on our FET devices is unlikely to change the back-gate capacitance of the device below the freezing temperature of the IL.[6] To further rule out the possibility of the IL droplet changing the back-gate capacitance in our graphene-contacted WSe_2 devices even below the freezing temperature of the IL, we have measured the transfer characteristics of a graphene FET fabricated on WSe_2 before and after depositing the IL. Figure S6 shows that the overall shape of the transfer curve of a graphene FET on the WSe_2 substrate does not change after depositing IL with the exception of the Dirac point, which is slightly shifted due to the small amount of IL-induced doping. This further confirms that the deposition of the IL on our devices does not change the back-gate capacitance.

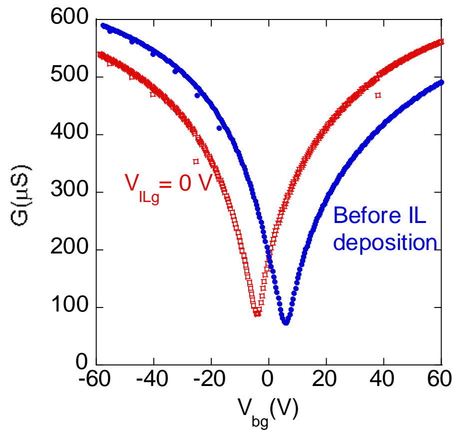

Figure S6. Conductance of a graphene FET device on WSe_2 substrate as a function of the back-gate voltage before and after deposition of the ionic liquid.

7. Change of the graphene work function caused by gating

The Fermi energy of a graphene monolayer changes as $\Delta E_F=(h/2\pi)v_F(\pi\ n)^{1/2}$, where v_F = 1.1×10^6 m/s is the Fermi velocity and n is the carrier density. The Fermi energy of a graphene monolayer is expected to be tunable by up to ±1.5 eV using an IL gate due to its extremely large electric double layer (EDL) capacitance. Such a wide range of Fermi energy tunability in graphene enables us to continuously change the work function of graphene from ~ 3 eV to ~6 eV, opening up the possibility of controllably making low-resistance Ohmic contacts with a vanishing or even negative Schottky barrier for both the electrons and holes in most semiconducting TMDs. In addition

to lowering the contact barrier at the graphene/TMD interface, the high carrier density induced by the IL gating is also expected to reduce the sheet resistance of graphene.

1. Li, X. S.; Cai, W. W.; An, J. H.; Kim, S.; Nah, J.; Yang, D. X.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; Banerjee, S. K.; Colombo, L.; Ruoff, R. S. *Science* **2009,** 324, (5932), 1312-1314.
2. Liang, X. L.; Sperling, B. A.; Calizo, I.; Cheng, G. J.; Hacker, C. A.; Zhang, Q.; Obeng, Y.; Yan, K.; Peng, H. L.; Li, Q. L.; Zhu, X. X.; Yuan, H.; Walker, A. R. H.; Liu, Z. F.; Peng, L. M.; Richter, C. A. *Acs Nano* **2011,** 5, (11), 9144-9153.
3. Tan, X.; Chuang, H.-J.; Lin, M.-W.; Zhou, Z.; Cheng, M. M.-C. *The Journal of Physical Chemistry C* **2013,** 117, (51), 27155-27160.
4. Ni, G.-X.; Zheng, Y.; Bae, S.; Tan, C. Y.; Kahya, O.; Wu, J.; Hong, B. H.; Yao, K.; Özyilmaz, B. *ACS Nano* **2012,** 6, (5), 3935-3942.
5. Xia, F.; Perebeinos, V.; Lin, Y.-m.; Wu, Y.; Avouris, P. *Nat Nano* **2011,** 6, (3), 179-184.
6. Perera, M. M.; Lin, M.-W.; Chuang, H.-J.; Chamlagain, B. P.; Wang, C.; Tan, X.; Cheng, M. M.-C.; Tománek, D.; Zhou, Z. *ACS Nano* **2013,** 7, (5), 4449-4458.