Supporting Information for

Low-Resistance 2D/2D Ohmic Contacts: A Universal Approach to High-Performance WSe_2, MoS_2, and $MoSe_2$ Transistors

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S1. Synthesis of bulk crystals of undoped WSe_2 and $MoSe_2$, Nb-doped WSe_2 and MoS_2, and Re-doped WSe_2

All TMD crystals (except undoped MoS_2 crystals, which were purchased from SPI Supplies) were synthesized by chemical vapor transport using iodine as transport agent. Single crystals of WSe_2 ($MoSe_2$) were grown as follows. Polycrystalline WSe_2 ($MoSe_2$) was first synthesized from a stoichiometric mixture of W (Mo) (Alfa-Aesar, 99.999%) and Se (Alfa-Aesar, 99.999%) powders. The mesh size is -22 for W (Mo) and -200 for Se. The starting materials were sealed in silica tubes under vacuum, and then slowly heated to 900 ^{o}C. The ampoules remained at 900^{o}C for seven days, and then were allowed to furnace cool to room temperature. Single crystals of WSe_2 ($MoSe_2$) were then grown using the polycrystals as starting material and iodine as a transport agent (~17.5 mg/cm^3 of iodine). The silica tubes containing phase-pure powder and iodine were sealed under vacuum and placed in a tube furnace with a 50^{o}C temperature gradient from the hotter end of the tube containing the charge (1050 ^{o}C) to the colder end where growth occurs (1000 ^{o}C). The silica tubes with the powder inside were evacuated, backfilled with argon, then again evacuated, backfilled with argon, and evacuated one last time before sealing. Crystals in the form of shiny silver plates with typical size 5 × 5 × 0.1 mm^3 grew over the course of 5 days. The as-grown crystals were phase-pure as determined by x-ray diffraction. For doped samples, 0.5% of Niobium (Rhenium) was used as substituent atoms for *p*-doping (*n*-doping), following similar procedure for growing undoped WSe_2 ($MoSe_2$) crystals. The only difference comes with the vapor transport. For the doped samples, the temperature gradient is from 1035^{o}C to 985^{o}C. In all cases, the heating rate was 1^{o}C/minute, the samples dwelled about 5 days, and then furnace cooled. The purity and mesh of the dopants are as follows: Nb = -325 mesh, 99.99% pure, metals basis excluding Ta (Ta ≤ 500ppm); Re = -22 mesh, 99.999% pure.

S2. Fabrication of ultrathin TMD field-effect transistors (FETs) with 2D/2D contacts and h-BN encapsulated channel

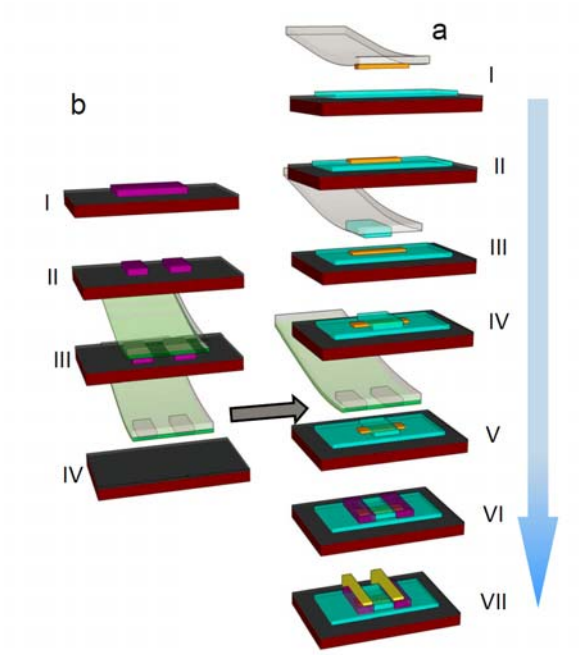

Figure S1. **Fabrication of TMD FETs with 2D/2D contacts and hBN encapsulated channel. a(I-II)** Exfoliate atomically thin TMD channel material onto a PDMS stamp and stack it on top of a thin bottom h-BN (10 - 30 nm) pre-transferred onto the SiO_2/Si substrate. **a(III- IV)** Exfoliate and transfer a thin top h-BN crystal (5 - 20 nm) to encapsulate the TMD channel. **a(V-VI)** Stack degenerately doped TMD electrodes on top of the exposed contact areas of the TMD channel to make 2D/2D drain/source contacts. **a(VII)** Deposit metal electrodes on top of doped TMD drain/source contacts. **b(I)** Degenerately doped TMD exfoliated on SiO_2/Si substrate. **b(II)** TMD drain/source electrodes defined by EBL and SF_6 dry etching. **b(III-IV)** Pick-up and transfer of the degenerately doped TMD electrodes for 2D/2D contact fabrication. Polycarbonate(PC)/PDMS double layer is used for the TMD electrode pick-up and subsequent transfer process.

Fig. S1 shows the process flow of the device fabrication. Thin h-BN crystals (10 - 40 nm thick) were produced from bulk h-BN crystals by a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrate covered with a 270 - 290 nm-thick thermal oxide layer. Atomically thin flakes of undoped TMDs (e.g. WSe_2 as shown in **Fig. 1** of the main text) were exfoliated from bulk crystals onto a PDMS stamp. Using a home-built precision transfer stage, undoped few-layer TMD flakes used as the channel were subsequently transferred onto selected thin h-BN

crystals on the SiO_2/Si substrate. To passivate the TMD channel, a second thin h-BN crystal is exfoliated to a PDMS stamp and subsequently transferred onto the few-layer WSe_2 flake to cover its middle section while exposing its two ends for electrical contacts. To make 2D/2D contacts, degenerately doped TMDs are exfoliated on to Si/SiO_2 substrates, patterned into drain/source electrodes by electron-beam lithography and SF_6 try etching, and transferred to the two exposed ends of the TMD channel as drain/source contacts using a pick-up method.[1-2] Alternatively, thin flakes of degenerately doped TMDs can be exfoliated onto PDMS stamps and transferred to the two exposed ends of the TMD channel as drain/source contacts, especially for long channel devices. To improve the interface quality between the h-BN and TMD channel as well as between the doped TMD drain/source contacts and TMD channel, a mild annealing step was carried out after each transfer step at 250 ^{O}C for 30 minutes in a vacuum chamber purged by 10% H_2 and 90 Ar. The dimensions (e.g. the sample thickness) and the surface quality (e.g. the cleanness and smoothness) of the h-BN substrate and TMD channel were characterized by Park Systems atomic force microscopy (AFM) in the non-contact mode after each annealing step. Metal electrodes, consisting of 5 nm of Ti covered by 50 nm of Au, were fabricated to electrically wire up the degenerately doped TMD drain/source electrodes using standard electron beam lithography (EBL) and electron beam deposition.

S3. Characterization of electrical contacts between metal (Ti/Au) and degenerately *p*-doped WSe_2

Fig. S2a,b shows I_{ds}-V_{ds} characteristics of a 12 nm thick degenerately *p*-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) device with Ti/Au contacts measured at 300 K and 10 K. The linearity of the I_{ds}-V_{ds} characteristics down to 10 K indicates ohmic behavior, which is ascribed to the highly transparent contacts between heavily doped WSe_2 and Ti/Au metal electrode. The I_{ds} only slightly increases as the gate voltage changes from 0 V to -80 V, indicating heavy *p*-doping. The I_{ds}-V_{ds} characteristics also show weak temperature dependence, indicating absence of carrier freeze-out, which is consistent with degenerate doping.

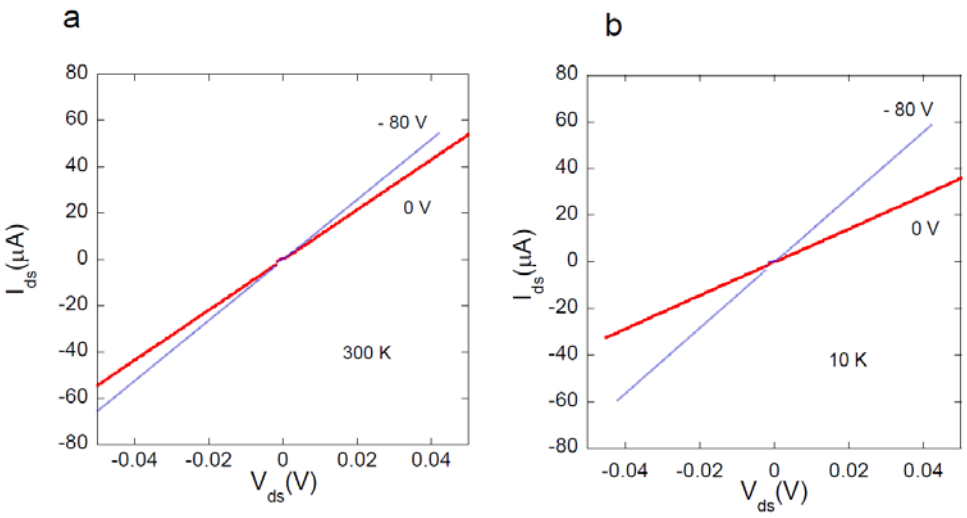

Figure S2. Output characteristics of a 12 nm thick Nb-doped WSe_2 with Ti/Au contacts measured at **a**, 300 K and **b,** 10 K. The linear I_{ds}-V_{ds} characteristics down to cryogenic temperatures indicate barrier-free ohmic behavior. The weak gate voltage dependence and weak temperature dependence of the drain-source current are consistent with degenerate *p*-doping.

Since the measured effective contact resistance R_C in **Fig. 2c** of the main text is the series resistance of metal contact resistance (R_{MC}), the layer resistance of the TMD drain/source ($R_{C\text{-}layer}$), the 2D/2D junction contact resistance ($R_{C\text{-}2D/2D}$), and the layer resistance of the channel material underneath the drain/source contacts ($R_{Ch\text{-}layer}$). In order to optimize the 2D/2D contacts, it is important to separately determine and optimize these constituent resistances. Particularly, it is important to determine R_{MC} , the contact resistance between the Ti/Au electrodes and degenerately *p*-doped WSe_2 . **Fig. S3a** shows a optical micrograph of a device structure used to extract the metal/*p*-doped WSe_2 contact resistance R_{MC}, where the channel length is defined as the spacing between adjacent Ti/Au metal electrodes. The total resistance measured between any adjacent pair of electrodes is the sum of contact resistance R_{MC} and channel resistance. By plotting the total resistance (multiplied by the channel width) as a function of channel length, both contact resistance and channel resistance can be separately determined for a uniform channel with consistent contacts. **Fig. S3b, c**

shows the normalized total resistance as a function of channel length for the device measured at room temperature and 5 K. From the intercept of the linear fit to the total resistance, we extract the contact resistance R_{MC} ~ 0.20 kΩ μm and 0.19 kΩ μm for room temperature and 5 K, respectively. Almost constant R_{MC} (0.18 - 0.20 kΩ μm) is observed for the entire temperature range between 5 K and 295 K, strongly indicating that the contacts between the degenerately *p*-doped WSe_2 and Ti/Au are ohimic, and have low contact resistance. The low R_{MC} is also expected to lead to high drive current. **Fig. S3d** shows the drain-source current as a function of drain-source voltage for a short channel of *p*-doped WSe_2 with a channel length of ~ 0.22 μm. The device exhibits a high drain current of > 1.5 mA/μm at V_{ds} = 2 V and V_{bg} = 0 V.

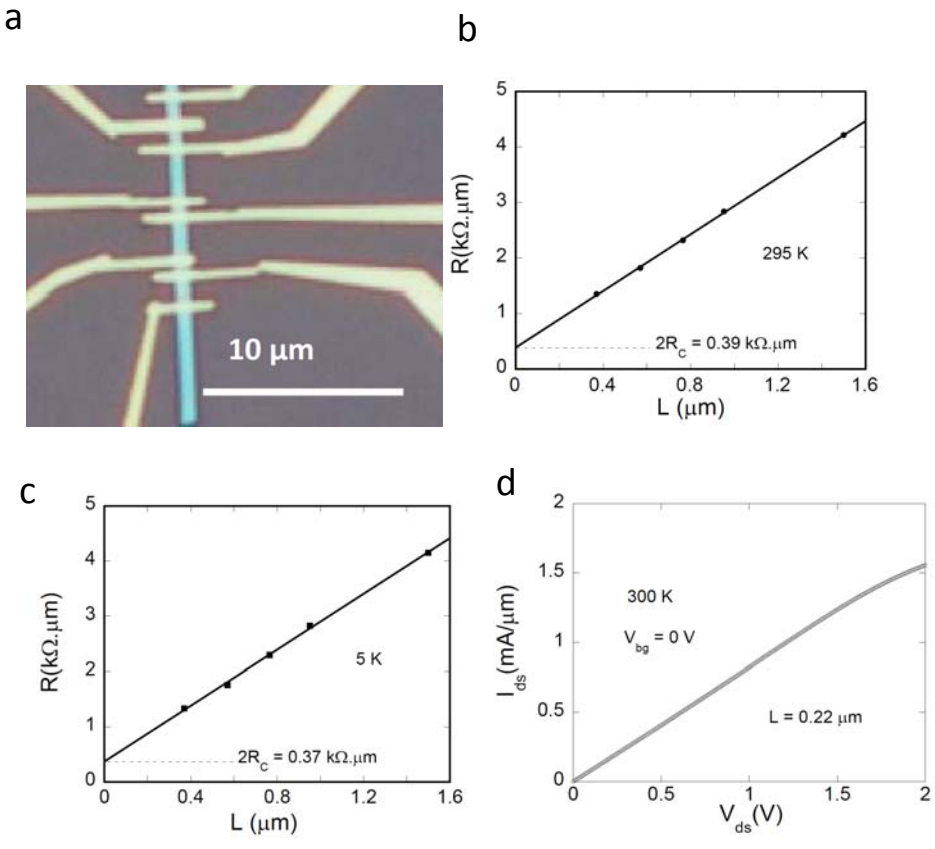

Figure S3. **a**, Optical micrograph of a device structure for TLM measurement consisting of a ~ 18 nm thick degenerately *p*-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) with

Ti/Au metal contacts. Normalized total resistance as a function channel length measured at room temperature **(b)**, and 5 K **(c)**. **d**, Drain-source current as a function of drain-source voltage at V_{bg} = 0 V.

S4. Contact resistance of WSe_2 2D/2D homo-contacts

Because the effective contact resistance R_C (~ 0.3 kΩ μm) extracted from the WSe_2 device in **Fig 2** of the main text also includes a metal/*p*-doped-WSe_2 contact resistance of ~ 0.2 kΩ μm, the actual 2D/2D contact resistance between degenerately p-doped WSe_2 drain/source and undoped WSe_2 channel is expected to be ~ 0.1 kΩ μm or less. Similar R_C is also achieved in another WSe_2 device with 2D/2D homo-contacts and a 9.2 nm thick channel. **Fig.S4 a, b** shows the optical micrograph of a 9.2 nm thick WSe_2 channel with degenerately *p*-doped WSe_2 2D/2D contacts and varying channel length between adjacent pairs of *p*-doped WSe_2 contacts. The top metal electrodes consist of 5 nm Ti and 50 nm Au. As shown in **Fig. S4c**, the normalized total resistance (multiplied by the channel width) increases linearly with the channel length. From the y intercept of the linear fit to total resistance, we extract a contact resistance of ~ 0.3 kΩ μm, in excellent agreement with the result in **Fig. 2c** of the main text. As the thickness of the channel increases, the gate field tuning of the channel Fermi level becomes less effective because of the increased screening of the gate field by the carriers in the channel.[3] As a result, the barrier at the 2D/2D interface between the degenerately doped drain/source and the channel cannot be completely eliminated in thicker samples, leading to a substantial increase of the 2D/2D interface resistance $R_{C\text{-}2D/2D}$. In addition, the layer resistance of the channel material underneath the drain/source contacts $R_{Ch\text{-}layer}$ is also expected to increase as the channel thickness increases. **Fig. S4c** shows the contact resistance R_C as a function of the WSe_2 channel thickness. When the channel thickness is below 10 nm, the effective contact resistance R_C is ~ 0.3 kΩ μm. As the channel thickness increases beyond 10 nm, the effective contact resistance increases rapidly with the channel thickness, reaching ~ 3 kΩ μm at a channel thickness of 30 nm due to the increased charge carrier screening and $R_{Ch\text{-}layer}$. Therefore, in order to obtain low 2D/2D contact resistance, it is crucial to

have a sufficiently thin channel (< 10 nm). However, as the thickness of the TMD channel reduces from few-layers to a monolayer, the valley degeneracy also decreases by a factor of three, leading to corresponding decrease of the density of states (DOS).[4] The reduced availability of states for charge injection in a monolayer TMD channel may lead to higher 2D/2D junction resistance and reduced drive current compared to multilayer channels.[5] Therefore, we focus on few-layer TMD channels in this study.

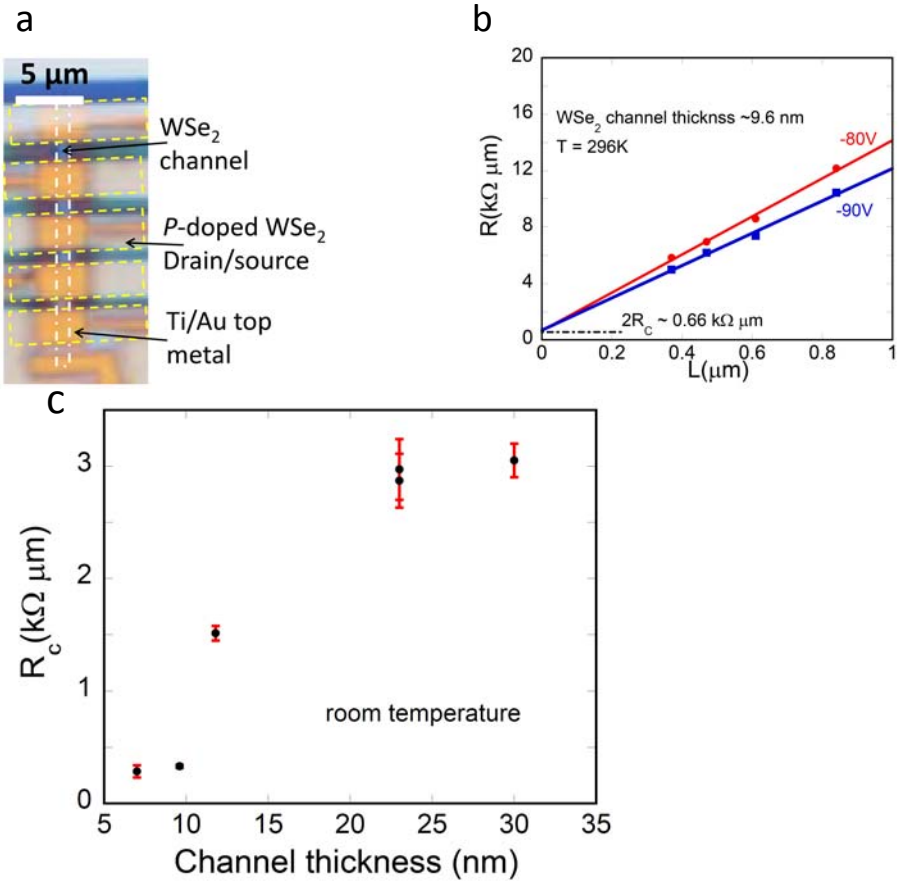

Figure S4. a, Optical micrograph of a 9.2 nm thick WSe_2 with 2D/2D homo-contacts for TLM measurement to determine the contact resistance **b,** Total resistance *R* (multiplied by the channel width) versus channel length *L*. The intercept of the linear fit on the vertical axis yields the contact resistance $2R_C$. **c**, Contact resistance as a function of the WSe_2 channel thickness.

S5. Transfer and output characteristics of a top-gated WSe_2 device with vertical 2D/2D contacts

Fig. S5 shows the transfer and output characteristics of a top-gated WSe_2 device with *p*-doped WSe_2 as drain and source contacts. In this device, a 10 nm thick h-BN crystal is used as the top-gate dielectric and Ti/Au is used as the top-gate electrode. A constant back-gate voltage is applied to electrostatically dope the WSe_2 in the 2D/2D contact region as well as in the under-lapped regions. As shown in **Fig. S5a**, the transfer characterizes at room temperature shows a near perfect subthreshold swing of 63 mV/dec, approaching the theoretical limit of ~ 60 mV/dec for an ideal MOSFET. As shown in **Fig. S5b**, the device exhibits clear current saturation at high drain/source voltages due to the channel pinch-off.

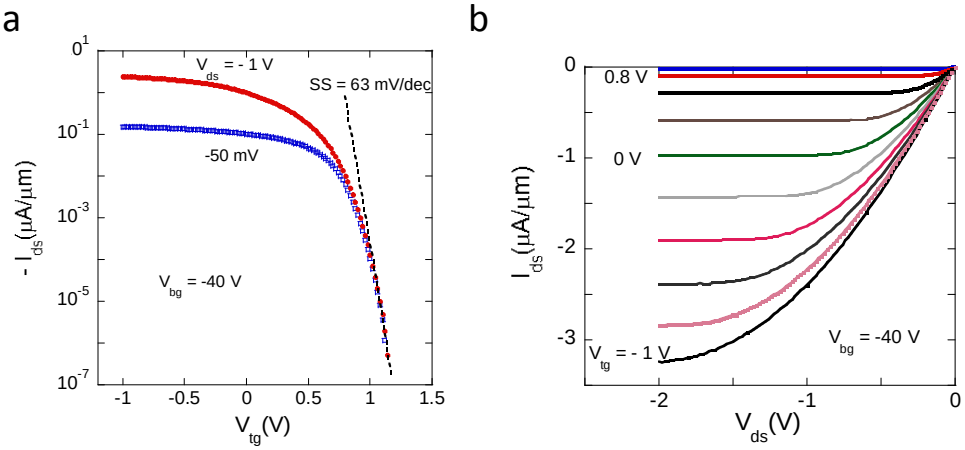

Figure S5. Room temperature transfer (**a)** and output (**b**) characteristics of a 3.5 nm thick WSe_2 device with degenerately *p*-doped WSe_2 as drain and source contacts. A back gate of - 40 V was applied to achieve ohmic drain/source contacts and turn on the underlap region between the top-gate electrode and drain/source contacts.

S6. Electrical characteristics of a *n*-type WSe_2 device with *n*-doped WSe_2 ($Re_{0.005}W_{0.995}Se_2$) as drain/source contacts

Fig. S6a,b shows the room temperature output and transfer characteristics of a WSe_2 device with degenerately *n*-doped WSe_2 as drain/source contacts. The device shows clear *n*-type behavior. As shown in **Fig. S6a**, the drain/source current is linear at all back gate voltages, indicating ohmic contacts. The transfer curve shows an on-off

ratio over 10^7 for electrons (**Fig. S6b**). The threshold voltage for the electron channel is much closer to zero than for the hole channel of WSe_2, suggesting that our WSe_2 crystals used as channel material are likely slightly *n*-dope.

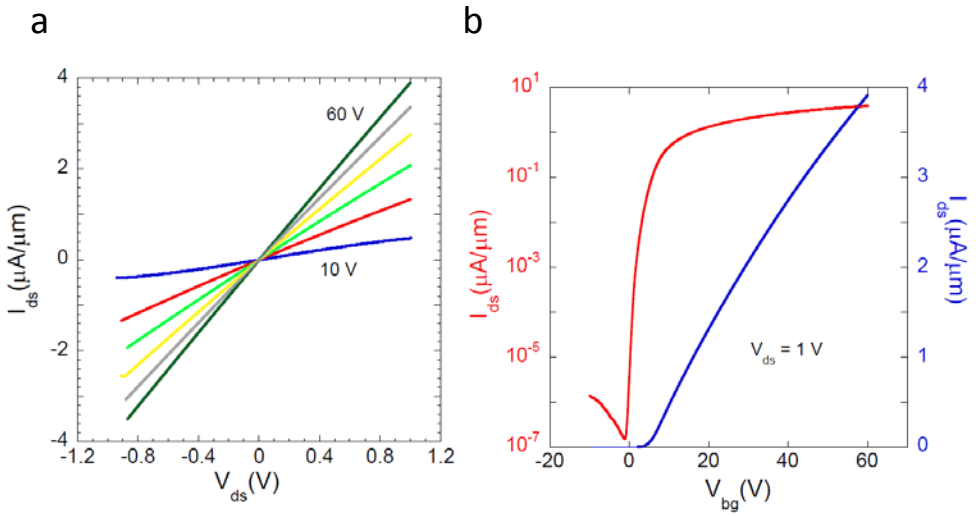

Figure S6. Room temperature output (**a)** and transfer (**b)** characteristics of a 8.5 nm thick *n*-type WSe_2 FET device with highly *n*-doped WSe_2 as drain/source contacts. Both linear and log plots are shown in **b**.

S7. Hysteresis-free transfer curves of a *p*-type WSe_2 with 2D/2D homo-contacts.

Fig. S7 shows the two-terminal conductivity as a function of gate voltage for the WSe_2 device in **Fig. 3** of the main text with the gate voltage being swept along both directions. The hysteresis is negligibly small at 300 K, which further decreases with decreasing temperature until it completely disappears below 80 K.

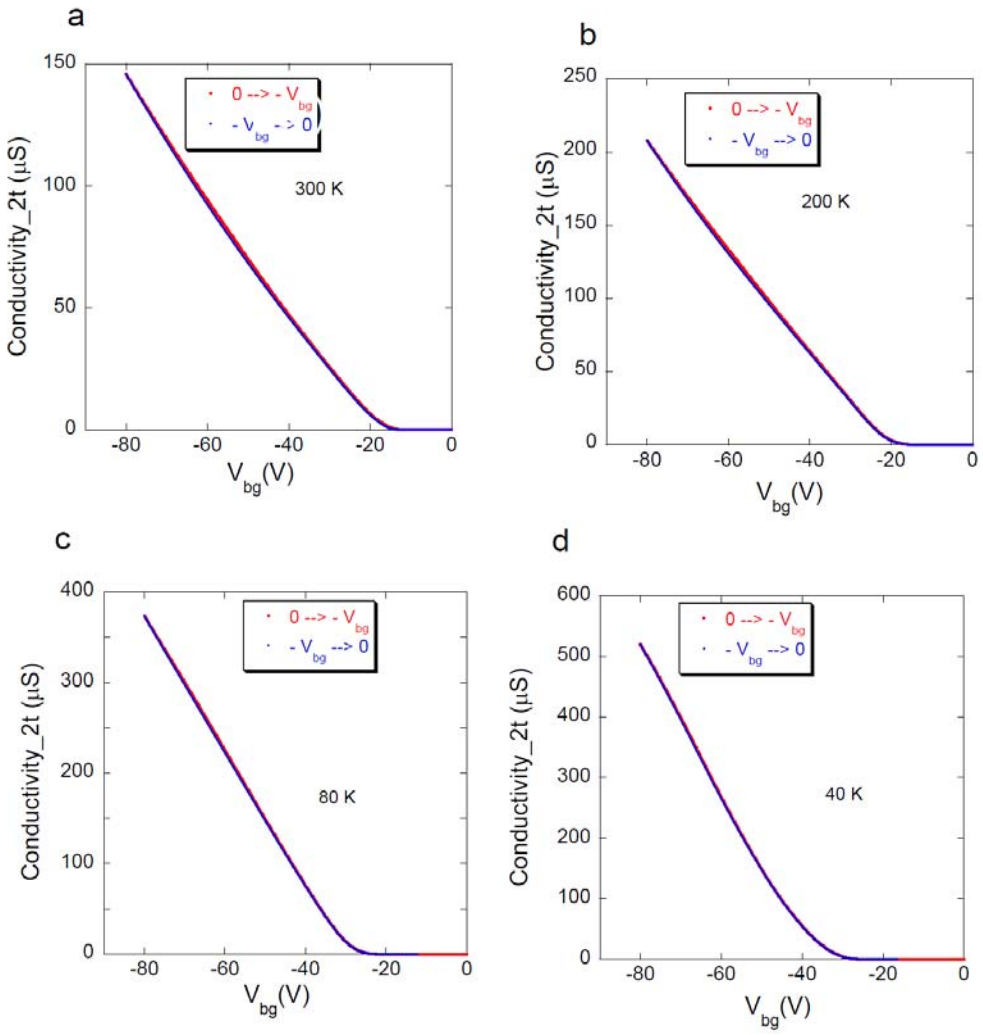

Figure S7. Transfer curves of the WSe_2 device shown in **Fig. 3** of the main text with opposite gate sweep directions measured at 300 K **(a)**, 200 K **(b)**, 80K (**c)** and 40 K (**d)**.

S8. Comparison of geometric back gate capacitance with the back gate capacitance determined by Hall effect measurement

Fig. S8a shows a Hall device with a WSe_2 channel encapsulated by h-BN from both top and bottom and on Si substrate with 285 nm of thermal oxide. The Hall bar structure was fabricated by placing degenerately *p*-doped WSe_2 thin flakes around the perimeter of an undoped WSe_2 flake sandwiched between a bottom h-BN substrate and a top h-BN that covers the center part of the TMD flake. 2D/2D contacts were

then formed between the degenerately *p*-doped WSe_2 flakes and the exposed edge areas of the undoped WSe_2 flake.[6] Subsequently, metal electrodes were fabricated on top of the *p*-doped TMD contacts, and the stack was shaped into a Hall bar geometry such that the h-BN encapsulated WSe_2 forms the channel. The WSe_2 channel is ~ 22 nm thick, and the top and bottom h-BN passivation layers are ~ 20 nm and ~ 30 nm thick, respectively. The geometric back gate capacitance of the device is calculated to be ~ 10.8 nF/cm^2 based the parallel plate capacitor model and a dielectric constant of 3.5 for h-BN.[7-8] We then performed Hall-effect measurement to determine the charge density as a function of gate voltage to extract the back gate capacitance. **Fig. S8b** shows the hole density determined by Hall measurement as a function of back gate voltage at 300 K. The slope of the gate dependence of hole density yields a back gate capacitance $C_{bg\text{-}Hall}$ = 9.8 nF/cm^2, which is in excellent agreement with the geometric capacitance.

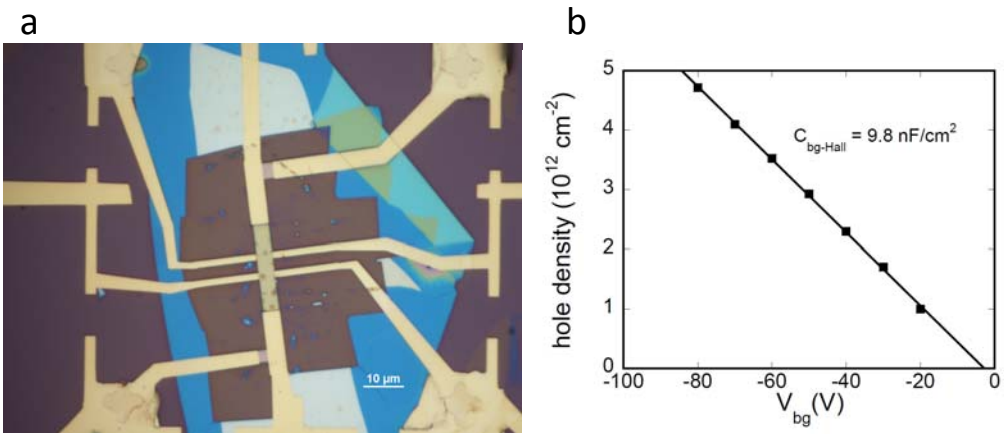

Figure S8. **a**, Optical micrograph of a h-BN encapsulated WSe_2 Hall bar device. **b**, Hole density extracted from Hall effect measurement as a function of back gate voltage at 300 K to determine the back gate capacitance.

S9. Summary of electrical characteristics of additional WSe_2 and MoS_2 devices with 2D/2D homo-contacts

Table S1

Device label	Channel/Contacts	Channel thickness (nm)	Length (μm)/ Width (μm)	μ_{FE} (cm^2/Vs) at RT and 80K	On/off ratio at RT V_{ds}=-1V
[2-15-15]_No3_04_12	WSe_2/*p*-WSe_2	4.0	5.3/8.4	170 (RT) 380(80 K)	10^7
[2-15-15]_No3_5-3_12	WSe_2/*p*-WSe_2	3.0	3.2/6.2	150 (RT) 490(80 K)	10^8
[3-23-15]_No1_2-5_12	WSe_2/*p*-WSe_2	10	20/1.8	200 (RT) 580(80 K)	10^6
[3-23-15]_No2_-2-5_12	WSe_2/*p*-WSe_2	10	37.4/5	240 (RT) 630(80K)	10^7
[4-4-15]_No3 -25_12	WSe_2/*p*-WSe_2	3.5	14.8/ 4.7	250 (RT) 620(80K)	10^9
[4-4-15]_No3 55_12	WSe_2/*p*-WSe_2	3.5	10.8/ 3.0	200 (RT) 540 (80K)	10^9
[5-29-15]_No.1 46_12	WSe_2/*p*-WSe_2	6.4	14.5/ 3.3	230(RT) 700(80K)	10^6
[7-12-15]_No.1 -60_12	MoS_2/*p*- MoS_2	6.8	13/2.7	180(RT) 550(80K)	10^7
[3-18-15]_No.3	MoS_2/*p*- MoS_2	18	10.5/ 4.4	120(RT)	10^6
[07-09-15]_No.1 -33_22	MoS_2/*p*- MoS_2	6.0	12.5/ 7.4	200(RT) 700(80K)	10^6

S10. Working principle of 2D/2D hetero-contacts of the devices in Fig. 4 of the main text.

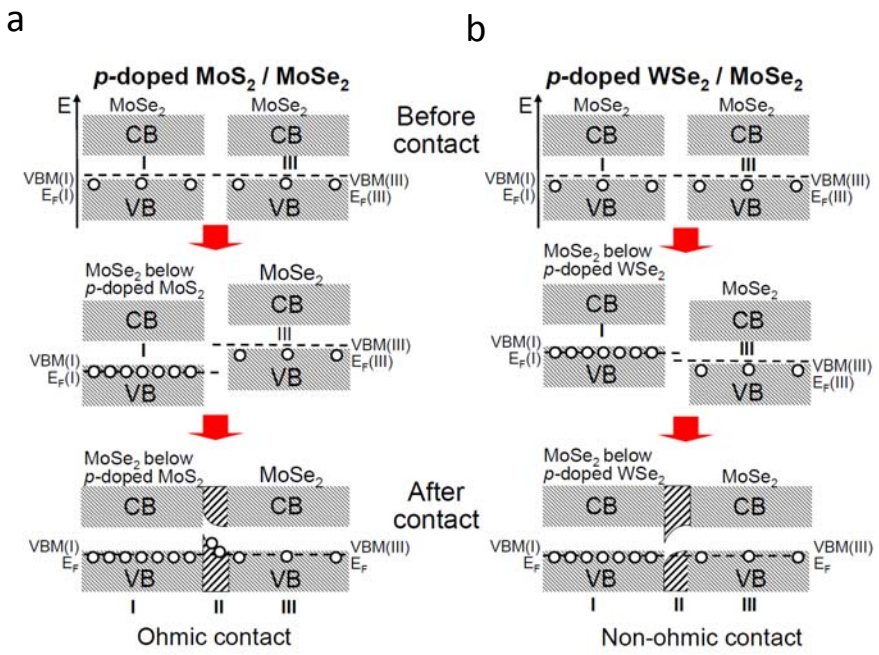

Figure S9. Working principle of 2D/2D hetero contacts. Changes in lateral band profiles induced by forming optimum 2D/2D heterojunctions in $MoSe_2$ contacted by *p*-doped MoS_2 ($Nb_{0.005}Mo_{0.995}S_2$) (**a**) and *p*-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) (**b**) .

The detailed working principle of the $MoSe_2$ devices with 2D/2D hetero-contacts, shown in **Fig. 4** of the main text, is schematically illustrated in **Fig. S9**. We will consider the channel material to be *p*-doped for simplicity, independent of its intrinsic behavior. This assumption is justified in *p*-type transistors, where the doping level is adjusted by a gate voltage during operation. In a Gedanken experiment, we physically separate the channel into two parts along the lateral direction, which we call regions I and III, and show the band diagram in the top panels of **Fig. S9a, b**. Next, we form a hetero-junction between the left segment of the channel, called region I, and the degenerately *p*-doped electrode material. Applying a gate voltage, we align the

valence band maximum (VBM) of the channel material with the VBM of the degenerately doped electrode material, which eliminates a contact barrier at the 2D/2D junction and increases the level of *p*-doping in the channel material in region I. As seen in the middle panels of **Fig. S9a and b**, this misaligns the VBMs and Fermi levels in region I and the separate region III. We conclude the Gedanken experiment by joining regions I and III. The Fermi level in the entire system must adjust to the same value of region I, given by that of the degenerately doped electrode. The band realignment occurs in the newly formed interface region II, as seen in the bottom panels of **Fig. S9a, b**.

Fig. S9a depicts the situation in a 2D/2D heterojunction formed of degenerately *p*-doped MoS_2 ($Nb_{0.005}Mo_{0.995}S_2$) as the contact material and undoped $MoSe_2$ in the channel. As indicated in the middle panel of **Fig. S9a**, this junction requires a down-shift of the energy levels in region III by approximately the difference of the VBM in regions I and III to align the Fermi levels. As a consequence, a local up-turn occurs in the valence band in region II. This is accompanied by a flow of holes from region I towards the interface region II. Hole accumulation in region II builds up a local electric field that eventually prevents further charge redistribution. The Fermi level is now unique and the junction shows ohmic behavior since hole accumulation in region II does not hinder hole transport.

Different behavior occurs at the interface between degenerately *p*-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) and $MoSe_2$. As seen in the middle panel of **Fig. S9b**, the VBM of the channel in optimum contact with the *p*-doped WSe_2 electrode in region I lies

above the VBM of $MoSe_2$ in region III. In this case, the valence band of the $MoSe_2$ channel bends downward at the lateral interface in region II, accompanied by a flow of holes away from this interface. Subsequent hole depletion in region II builds up a local electric field that eventually stops further charge redistribution. The Fermi level is now unique, but the junction shows non-ohmic behavior since hole depletion in region II acts as a barrier hindering hole transport.

S11. Electrical characteristics of additional MoS_2 and WSe_2 channel devices with 2D/2D hetero-contacts

Figure S10a shows the transfer characteristics of a MoS_2 channel contacted by degenerately *p*-doped WSe_2 drain/source contacts measured at different temperatures. Similar to $MoSe_2$ devices with *p*-doped WSe_2 contacts, the two-terminal conductivity decreases with decreasing temperature, indicating the presence of a contact barrier, which can be attributed to the formation of a lateral depletion region because the VBM of MoS_2 lies below the VBM of WSe_2. As shown in **Fig. S10b**, the two-terminal conductivity of a WSe_2 with degenerately *p*-doped MoS_2 drain/source contacts shows a metal insulator transition and the conductivity increases with decreasing temperature in the metallic regions, indicating ohmic contacts. Similar to the case of $MoSe_2$ contacted with *p*-doped MoS_2, a lateral accumulation region is formed near the drain/source contacts, leading to ohimic behavior.

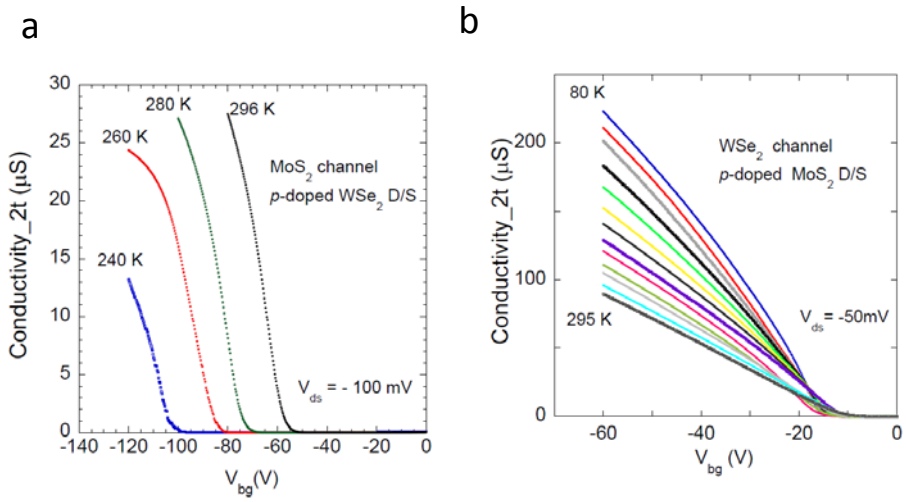

Figure S10. Two-terminal conductivity of a MoS_2 channel device with degenerately *p*-doped WSe_2 drain/source contacts **(a)**, and a WSe_2 channel device with degenerately *p*-doped MoS_2 drain/source contacts **(b)**.

S12. Comparison of the electrical characteristics of a WSe_2 measured 3 weeks apart

Fig. S11 shows the two-terminal conductivity as a function of gate voltage of a hBN encapsulated WSe_2 device with 2D/2D homo-contacts measured at 300 K in the PPMS. No significant difference is observed between the original measurement and a measurement after three weeks of air exposure, indicating excellent air stability of the device.

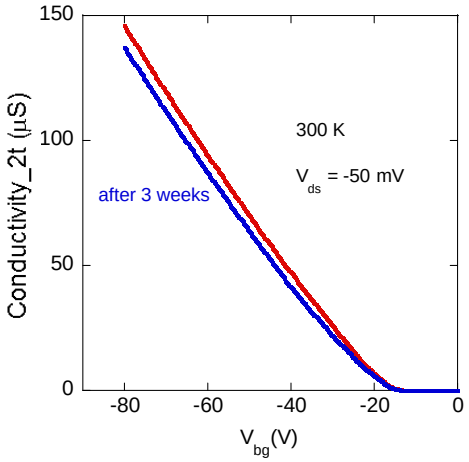

Figure S11. Transfer curves of a WSe_2 devices with degenerately *p*-doped WSe_2 drain/source contacts measured three week apart.

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